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A novel SRAM test method based on embedded implementation on FPGA

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Abstract：With the development of satellite based remote sensors, embedded systems become more and more popular in space camera electronics. Static Random Access Memory(SRAM) is one kind of the most widely used memories due to its merits of high efficiency and low power dissipation, but testing its function still depends on writing testing modules with hardware description language, which results in low developing efficiency and low reliability. In this paper, an embedded testing method is proposed, which is based on MicroBlaze and its speed increasing function design. Implementation of the test method is based on reusable Intellectual Property(IP) technique and greatly improves data transfer speed. With this method, secondary development of SRAM test system can be made in application layer instead of fundamental logical layer, which simplifies the system design. It is not only more efficient and more reliable, but also easier to transplant, which greatly reduces test design cost. The validity and feasibility of the method have been proved by test results.

Key words：Static Random Access Memory；Field Programmable Gate Array；embedded system；reliability；high-speed circuits

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With the demanding requirements, development for real-time transferring space camera electronics become more and more challenging. SRAM(Static RAM) is widely used in space camera electronics because the use of SRAM is easier and more reliable[1] compared with other memories. As there is an increasing demand for the use of SRAMs in embedded systems, shortening the test period of SRAM has great significance for the whole project schedules.

Test methods for SRAM still depend on writing test module with Very High speed integrated circuit hardware Description Language(VHDL). These traditional methods have disadvantages of long development period, low testing efficiency and low reliability, etc[2]. Therefore, we need to develop new test methods that can shorten test cycle, with high-efficiency and good reliability, especially in space field which has strict requirements for the system and components. Embedded system design is promising for aero-control system as it has characteristics of simple hardware circuit, high integration and low system power dissipation[3].

In this paper, we propose an embedded implementation of SRAM interface based on MicroBlaze and its speed increasing function design. Compared with traditional methods, the proposed method focuses on the design of functional application layer instead of fundamental hardware module. At the same time, an embedded test system can be configured through graphical interface, and it is easy to migrate to different SRAMs. Moreover, the adopted IP core(Intellectual Property Core) is commercial and has passed a complete test procedure, which ensures more reliability. Therefore, the method in this paper can greatly reduce test design risk, shorten test design cycle and lower production costs.

1　Embedded System Design

1.1 Develop Procedure

In this paper, the developed embedded system is taken as a subsystem of the top-level FPGA design, which sufficiently uses the hardware resource of FPGA, and is liable to satisfy the functional requirements of plane-focused program.

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The developing procedure is shown in Fig.1, and Integrated Software Environment(ISE) 13.2 design suite is adopted as the developing tool, including ISE, Xilinx Platform Studio(XPS), Software Development Kit(SDK) and Chipscope. An embedded design procedure is comprised of hardware/software design and debug. XPS is used for hardware design, SDK is for software design, ISE is for top-level design, and Chipscope is for debugging.

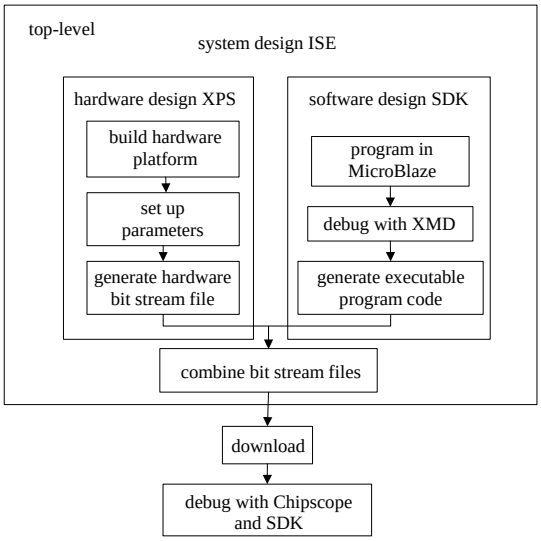

Fig.1 Developing procedure of embedded design

In this paper, down-top design method is adopted. First, establish the embedded hardware platform in XPS, including establishing hardware platform, setting up parameters and generating hardware bit stream. Second, design software in SDK, including programming in MicroBlaze, debugging and generating executable program code. Third, implant the embedded system as a submodule of top-level system in ISE, including adding an embedded system file of xmp format and an executable file of elf format, connecting embedded system modules and adding design constraints. At last, execute debugging with SDK and Chipscope[4].

1.2 Structure of Embedded System

In this paper, the embedded system is composed of Micro Control Unit (MCU), memory, peripherals, IO ports, etc. Almost all the necessary interface modules are already implanted in an FPGA, so design of the embedded system is realized by correctly connecting needed IP cores. Implementation of the embedded SRAM interface is also based on reusable IP technique. The MicroBlaze of Xilinx is MCU. PLB is the bus to interact with peripherals. The interface with SRAM is realized by EMC IP core. The structure of the embedded system is shown in Fig.2.

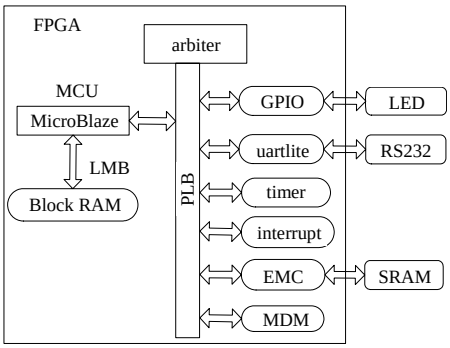

Fig.2 Structure of embedded system

MicroBlaze is a microprocessor IP core of Xilinx, which adopts RISC structure and 32 bit Harvard instruction bus and data bus. An evident advantage of this structure is that a whole embedded system can be realized by connecting necessary IP cores, which makes it easily to simplify system and effectively utilize resources, therefore, this structure has characteristics of good compatibility, design flexibility and reusability[5].

Two buses are utilized in the design. One is synchronized LMB bus, which adopts simple protocol that data in on-chip RAM can be read and written in one clock period. It is used to connect MicroBlaze and BRAM(Block RAM). The design in this paper doesn't need extra off-chip memory. The other is 128 bit PLB bus, which connects several master and slave peripherals to the embedded system. Besides EMC core, a UART core is added to interact with HyperTerminal, a GPIO core is for LED, a DMA core is for speed acceleration, a TIMER core is used to measure the speed, and an INTERRUPT core is for interrupt control of different IP cores.

SRAM used in this paper is 3DSR16M, its timing diagram of read and write cycle is shown in Fig.3 and its ports are described in Table1.

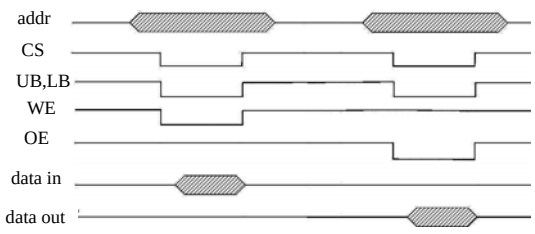

Fig.3 Timing diagram of read/write cycle

Table1 SRAM ports definition

port	description
D	bidirectional data bus, 16 or 32 bit
A	address input, 18 bit
CS0/CS1	chip selection signal, active low.
OE	output enable signal, active low
WE	write enable signal, active low
UB/LB	enable upper or lower bits, decide data width.

Controlled by signals UB, LB, it extends the width of data-bus by connecting two 16 bit chips in parallel, and the SRAM expands capacity through signals CS0, CS1, which is shown in Fig.4.

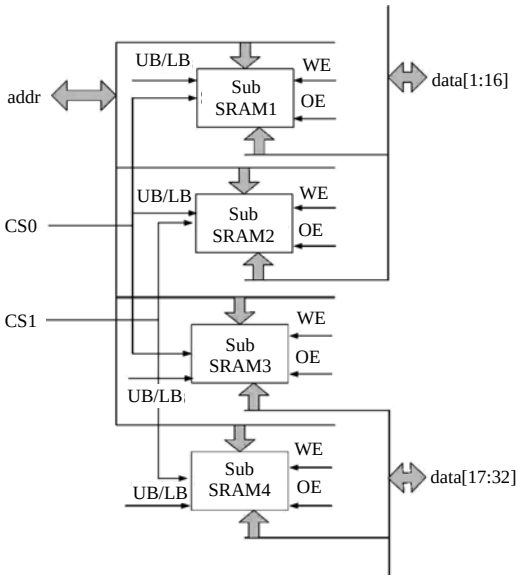

Fig.4 Schematic diagram of the SRAM

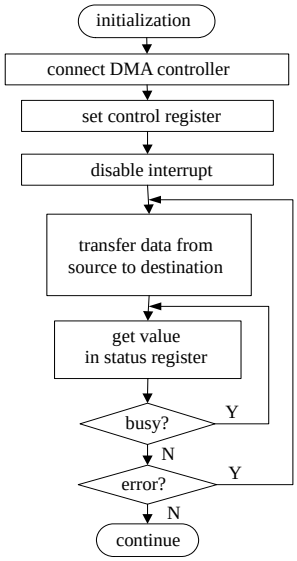

Fig.5 Diagram of software program

1.3 Program Design

Following the diagram in Fig.5, all needed IP cores are integrated in the software program.

The Xilinx External Memory Controller (EMC) provides the control interface for external SRAM memory through PLB. It is connected as a 32 bit slave on PLB bus. EMC core supports both single-beat and burst transaction modes, and the transferred data width can be designed as 32 bit, 16 bit or 8 bit. The cycle time for read and write operations can be configured. Port definitions of EMC core are shown in Table2. SRAM and EMC core are connected as shown in Fig.6.

Table2 Ports definition of EMC core

port	direction	definition
RdClk	I	read clock
MEM_DQ	IO	data bus
MEM_A	O	address bus
MEM_CEN	O	chip enable signal, active low
MEM_OEN	O	output enable signal, active low
MEM_WEN	O	write enable signal, active low

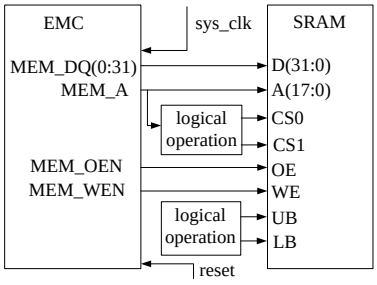

Fig.6 Connection between SRAM and EMC

In the design, UB and LB are set as low level. An extra bit of address bus is connected to chip selection bit to expand capacity. Considering requirements of configuration parameters and the fact that data of PLB bus is big-endian, while that of SRAM is little-endian, the data signals and address signals are connected as Table3 shows.

Table3 Connection of bus and data signals

signal	EMC core	SRAM
data bus	MEM_DQ (0:31)	D(31:0)
address bus	MEM_A (12:29)	A(17:0)

The XPS Direct Memory Access(DMA) Controller, which is connected as a 32 bit slave on PLB bus, provides direct data transmission for peripherals and memory devices on the PLB[6]. The controller transfers a programmable quantity of data from a source address to a destination address without processor intervention, and it supports burst transaction[7].

With SRAM connected with the system through the embedded method, users even do not need to care about the data width of SRAM. Programmed with proper configuration, the system finishes read and write process automatically

According to the given address and data.

In this paper, we test the system preliminarily. The data read from SRAM with the original data written in before have been compared. Based on this, other SRAM functional testing methods can be realized through software program easily.

2 Test Results

The performance of the embedded system has been tested. The test board is shown in Fig.7, where FPGA is Virtex4. The reference clock frequency of MicroBlaze is set to 100 MHz, coinciding with that of the on-board oscillator. Considering speed requirements of SRAM, the system clock frequency is set to 50 MHz. Test results show that the system can read and write data correctly, which proves the correctness and feasibility of the proposed embedded accelerating method.

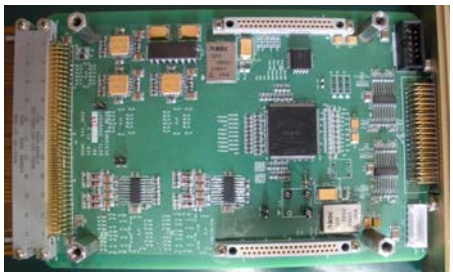

Fig.7 Test board

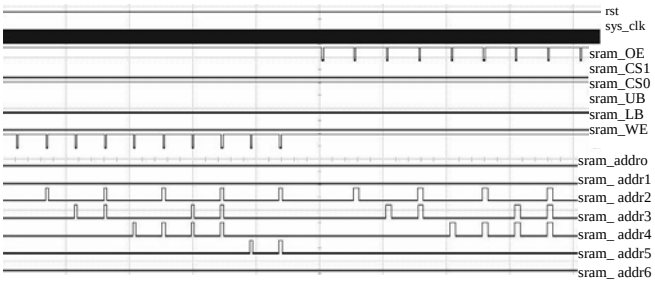

Fig.8 Timing of SRAM interface in oscillograph

In the experiment, a great deal of data is written in SRAM through EMC in different modes, and writing speed is tested with TIMER core. Then, data is read back and reading speed is tested. The timing of SRAM interface is captured with Agilent mixed oscillograph MS09104A, as is shown in Fig.8.

Comparing of data transfer speed in different modes is listed in Table4. Reading or writing a 32 bit data through writing test module method needs one clock period, but through embedded software programming method, reading a 32 bit data needs 43 clock periods, while writing needs 39 clock periods. Reading or writing speed is the fastest through embedded DMA method, which needs 0.6 clock period on average. Test results show that the proposed design is not only feasible, but also very efficient.

Table4 Comparison of data transfer speed

data transfer mode	reading speed (clock period)	writing speed
test module with VHDL	1.0	1.0
embedded software programming mode	43.0	39.0
embedded DMA mode	0.6	0.6

Table5 Comparison of different design methods

performance	VHDL design	embedded design
reliability	inadequate test	commercial, mature IP core, reliable
efficiency	design cycle: about 1 month	less code, more effective
compatibility	specialized, poor compatibility	easy to configure and modify, good compatibility

As is shown in Table5, traditional methods take about a month to develop testing interface module using VHDL, and it is hard to test the reliability of the testing module. Furthermore, the module needs to be redeveloped totally in face of different requirements, which not only demands a long design and test cycle again, but also is fallible. Compared with the traditional methods, the proposed method uses mature commercial IP cores, which are reliable. If needed, modifications are made in application layer instead of fundamental logical layer, which simplifies the system design. Therefore, the proposed method has the advantages of shorter design cycle and better compatibility, which decreases cost greatly, improves system performance and has better reliability.

3 Conclusion

SRAM is widely used in aerospace electronics, including real-time transporting space cameras. In this paper, an embedded implementation of SRAM interface and its speed acceleration method are presented, which provides a new

method for its functional test. Test results demonstrate the feasibility and effectiveness of this method. The proposed method also provides a new testing method for other electronic components. To apply embedded design technique in space camera electronics can not only make better use of resources in FPGA, but also meet the demands of reusability and revisability for the system, thus it has a promising future in aerospace electronics.

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基于 FPGA 嵌入式的 SRAM 测试方法

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摘　要：随着航天技术的发展，嵌入式系统设计在航天上得到了越来越广泛的应用。静态随机存储器(SRAM)作为使用最为广泛的存储器之一，由于其高速低功耗的优良特性，在航天领域被广泛使用。目前，其功能测试还依赖于通过使用 VHDL/Verilog 编写测试端口来完成，不仅开发效率低，而且很难保证测试结果的可靠性。本文提出了一种通过嵌入式开发的方式完成对静态随机存储器(SRAM)功能测试的方法，测试方法基于可复用的 IP 技术，大大提高了测试数据传输效率。通过这种方法，SRAM 测试系统的二次开发基于应用层而不是底层逻辑层，大大简化了系统设计。这样不仅提高了测试效率，而且具有较好的可靠性、可配置性以及可移植性，大大降低了系统的研发成本。测试系统的可行性和有效性已经得到了实验验证。

关键词：静态随机存储器；现场可编程门阵列；嵌入式；可靠性；高速电路